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PTO/SB/21 (09-06)

Approved for use through 03/31/2007. OMB 0651-0031

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		Patent Number	7,049,526				
TRANSMITTAL			Issue Date	March 23, 2006			
	FC)RM		First Named Inventor	Jones, C	Christopher C.	
,			Art Unit	2841			
(to be used for all	corres	pondence after initial fi	ling)	Examiner Name	Semenenko, Yuriy		
Total Number of Pa	ages ir	This Submission	6	Attorney Docket Number	P17172		
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37 CF	FR 1.5	52 or 1.53				of	Correction
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Firm Name	Buc	kley_Maschoff & Ta	lwalkar	rrc			
Signature		1/1/21		7			
Printed name Nandu A. Talwalkar							
Date April 5, 2007		Reg. No. 41,339)			
			CDTIC:	ICATE OF TRANSMISSION	1/84 A 11 151		
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: JONES et al.

Patent No.: 7,049,526

Issue Date: March 23, 2006

For: MICROVIA STRUCTURE AND

FABRICATION

Confirmation No.: 4178

Group Art Unit: 2841

Examiner: Semenenko, Yuriy

REQUEST FOR CERTIFICATE OF CORRECTION Under 37 CFR § 1.322

Docket No.: P17172

Buckley, Maschoff & Talwalkar LLC

Attorneys for Intel Corporation

50 Locust Avenue

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CERTIFICATE OF MAILING UNDER 37 CFR 1.8

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Alexandria, VA 22313-1450

Sir:

The above-identified Letters Patent includes errors reflecting no fault on the Applicants' part. Specifically, the Letters Patent does not reflect the Examiner's Amendment set forth in the March 10, 2006 Notice of Allowability. The enclosed Certificate of Correction is believed to remedy this error and grant thereof is respectfully requested.

Patent No.: 7,049,526 Docket No.: P17172

The Commissioner is hereby authorized to charge any additional fees that may be required, or credit any overpayment, to Deposit Account <u>50-1852</u>.

Respectfully submitted,

April 5, 2007 Date

Nandu A. Talwalkar Registration No. 41,339

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UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

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PATENT NO.

: 7.049,526

APPLICATION NO.: 10/700,209

ISSUE DATE

: 5/23/2006

INVENTOR(S)

: Jones, et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

9. A method comprising:

fabricating a first metallization layer comprising a first microvia pad; and fabricating a second metallization layer comprising a second microvia pad wherein the [a] microvia pad having a base and a projection extending from the base; and

fabricating an intermediate layer disposed between the first metallization layer and the second metallization layer, the intermediate layer comprising a microvia electrically coupled to the first microvia pad and to the second microvia pad wherein the [a] microvia having plurality of surfaces facing a plurality of surfaces of the projection.

10. [A] The method according to Claim 9, further comprising:

fabricating an electroless conductor disposed between the microvia and the microvia pad, wherein the microvia pad and the microvia are composed of an electrolytic conductor.

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PATENT NO.

: 7.049.526

APPLICATION NO.: 10/700,209

ISSUE DATE

: 5/23/2006

INVENTOR(S)

: Jones, et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

11. [A] The method according to Claim 10, wherein fabricating the microvia pad comprises:

fabricating the base; and

fabricating the projection extending from the base after fabricating the base.

12. A system comprising:

an integrated circuit package comprising:

a first metallization layer comprising a first microvia pad;

a second metallization layer comprising a second microvia pad having a projection extending in a direction toward the first microvia pad; and

an intermediate layer disposed between the first metallization layer and the second metallization layer, the intermediate layer comprising a microvia electrically coupled to the first microvia pad and to the second microvia pad; and

a double data rate memory electrically coupled to the integrated circuit package.

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PATENT NO. : 7,049,526 APPLICATION NO. : 10/700,209 ISSUE DATE : 5/23/2006

: Jones, et al.

INVENTOR(S)

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

- 13. [A] <u>The</u> system according to Claim 12, wherein the microvia includes a plurality of surfaces facing a plurality of surfaces of the projection.
- 14. [A] <u>The</u> system according to Claim 12, wherein the projection is an integral portion of the second microvia pad.
- 15. [A] <u>The</u> system according to Claim 12, further comprising: a motherboard electrically coupled to the integrated circuit package and to the memory.

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